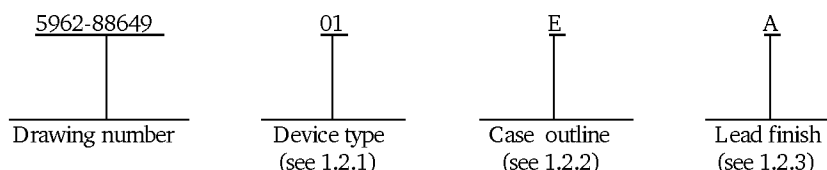


REVISIONS																			
LTR	DESCRIPTION										DATE (YR-MO-DA)					APPROVED			
A	Changes in accordance with NOR 5962-R118-92.										92-02-04					M. A. Frye			
B	Changes in accordance with NOR 5962-R198-93										93-07-13					M. A. Frye			
C	Incorporate revisions A and B N.O.R.'s. Update drawing to current requirements. Editorial changes throughout. - drw										01-08-15					Raymond Monnin			
D	Corrected generic number paragraph 1.2.1. -drw										02-10-04					Raymond Monnin			
<p>THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED</p>																			
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REV STATUS					REV		D	D	D	D	D	D	D	D	D	D	D		
OF SHEETS					SHEET		1	2	3	4	5	6	7	8	9	10	11	12	
PMIC N/A					PREPARED BY					DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.d sec.dla.mil									
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A					CHECKED BY														
					APPROVED BY														
					DRAWING APPROVAL DATE														
					Larry T. Gauder Ray Monnin Michael A. Frye 88-11-17 D					SIZE		CAGE CODE		5962-88649					
										A		67268							
										SHEET 1 OF 12									

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	55ALS195	Quadruple differential line receiver with three-state outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line
F	GDIP2-F16 or CDFP3-F16	16	flat pack
2	CQCC1-N20	20	square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage, A or B inputs	-15 V dc to +15 V dc
Differential input voltage ¹ / ₂	-15 V dc to +15 V dc
Enable input voltage	-1.5 V dc to +7.0 V dc
Low level output current	50 mA
Maximum power dissipation (P _D) ² / ₂	192.5 mW
Storage temperature range	-60 °C to +150 °C
Lead temperature (soldering, 60 seconds)	+260 °C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835
Junction temperature (T _J)	+150 °C

1.4 Recommended operating conditions.

Supply voltage range (V _{CC})	4.5 V dc minimum to 5.5 V dc maximum
Common mode input voltage (V _{CM})	±7.0 V dc maximum
Differential input voltage (V _{ID})	±12.0 V dc
High level input voltage (V _{IH})	2.0 V dc minimum
Low level input voltage (V _{IL})	0.8 V dc
Maximum high level output current (I _{OH})	-0.4 mA
Maximum low level output current (I _{OL})	16 mA
Case operating temperature range (T _C)	-55 °C to +125 °C

¹/ Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

²/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short circuit test, e.g., I_{OS}.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks . The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence . In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements . The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer List (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions . The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines . The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections . The terminal connections shall be as specified on figure 1.

3.2.3 Truth table . The truth table shall be as specified on figure 2.

3.2.4 Logic diagrams . The logic diagrams shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms . Test circuit and switching waveforms shall be as specified on figure 4.

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3.3 Electrical performance characteristics . Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements . The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking . Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark . A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance . A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

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3.7 Certificate of conformance . A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change . Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review . DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection . Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening . Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C T_C +125°C 4.5 V V_{CC} 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Positive-going threshold voltage	V_{T+}		1, 2, 3	All		200	mV
Negative-going threshold voltage	V_{T-}		1, 2, 3	All	-200		mV
Enable input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$	1, 2, 3	All		-1.5	V
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}$, $V_{ID} = 200 \text{ mV}$, $I_{OH} = -0.4 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$	1, 2, 3	All	2.5		V
Low level output voltage	V_{OL}	$V_{ID} = -200 \text{ mV}$, $V_{IH} = 2.0 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $V_{CC} = 4.5 \text{ V}$	1, 2, 3	All		0.45	V
						0.50	
High impedance state output current	I_{OZ}	$V_{CC} = 5.5 \text{ V}$, $V_{IL} = 0.8 \text{ V}$	1, 2, 3	All		20	μA
						-20	
Line input current	I_I	Other input at 0.0 V	1, 2, 3	All		1.2	mA
						-1.7	
High level enable input current	I_{IH}	$V_{CC} = 5.5 \text{ V}$	1, 2, 3	All		20	μA
						100	
Low level enable input current	I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IL} = 0.4 \text{ V}$	1, 2, 3	All		-100	μA
Input resistance	R_I	$V_{CC} = 5.5 \text{ V}$	1, 2, 3	All	12		k
Short circuit output current	I_{OS}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0.0 \text{ V}$, $V_{ID} = 3.0 \text{ V}$, $\frac{1}{\text{L}}$	1, 2, 3	All	-15	-130	mA
Supply current	I_{CC}	$V_{CC} = 5.5 \text{ V}$, outputs disabled	1, 2, 3	All		35	mA
Functional tests		See 4.3.1c	7, 8	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55°C T _C +125 °C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Propagation delay time, A, B to Y	t _{PLH}	V _{CC} =4.5 V to 5.5 V, V _{ID} =-1.5 V to 1.5 V, C _L =15 pF, See figure 4 2/	9	All		25	ns	
			10, 11	All		35	ns	
	t _{PHL}		9	All		23	ns	
			10, 11	All		34	ns	
Output enable time, A, B to Y	t _{PZH}		V _{CC} =4.5 V to 5.5 V, C _L =15 pF, See figure 4 2/	9	All		28	ns
				10, 11	All		40	ns
	t _{PZL}			9	All		27	ns
				10, 11	All		40	ns
Output disable time, A, B to Y	t _{PHZ}	V _{CC} =4.5 V to 5.5 V, C _L =15 pF, See figure 4 2/		9	All		30	ns
				10, 11	All		40	ns
	t _{PLZ}			9	All		24	ns
				10, 11	All		35	ns

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition shall not exceed one second.

2/ Vendor may test with V_{CC} =5.0 V but must guarantee the 4.5 V to 5.5 V limits.

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Device type	01	
Case outlines	E and F	2
Terminal number	Terminal symbol	
1	1B	NC
2	1A	1B
3	1Y	1A
4	1, 2EN	1Y
5	2Y	1, 2EN
6	2A	NC
7	2B	2Y
8	GND	2A
9	3B	2B
10	3A	GND
11	3Y	NC
12	3, 4EN	3B
13	4Y	3A
14	4A	3Y
15	4B	3, 4EN
16	V _{CC}	NC
17	---	4Y
18	---	4A
19	---	4B
20	---	V _{CC}

NC =No internal connection

FIGURE 1. Terminal connections .

Differential input	Enables	Output
A - B	EN	Y
V _{ID} 0.2 V	H	H
-0.2 V <V _{ID} <0.2 V	H	I
V _{ID} -0.2 V	H	L
X	L	Z

H =High level voltage

L =Low level voltage

X =Irrelevant

I =Indeterminate

Z =High impedance (off)

FIGURE 2. Truth table .

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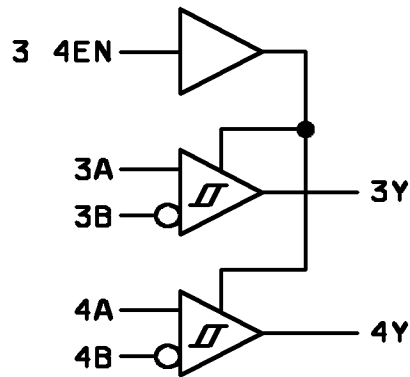
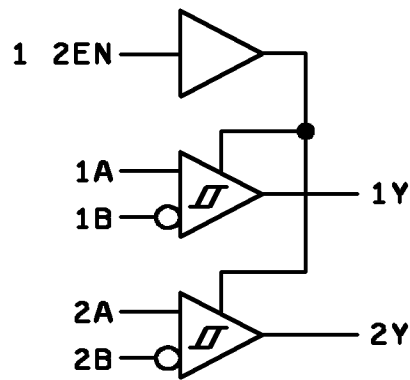
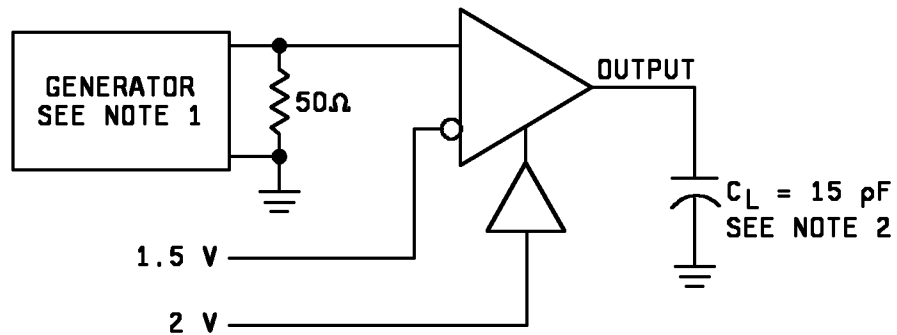


FIGURE 3. Logic diagram .

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TEST CIRCUIT

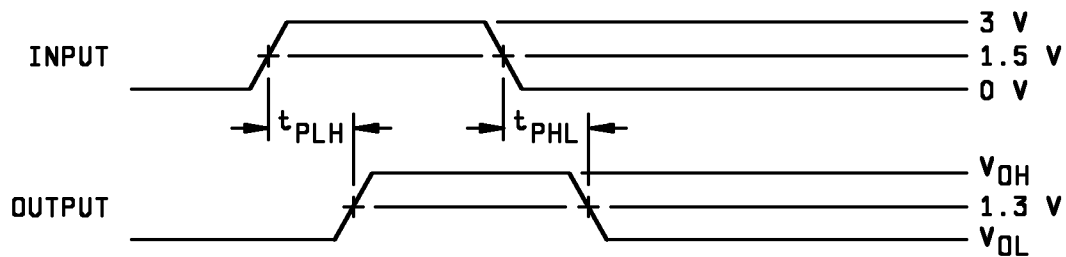


FIGURE 4. Test circuit and switching waveforms.

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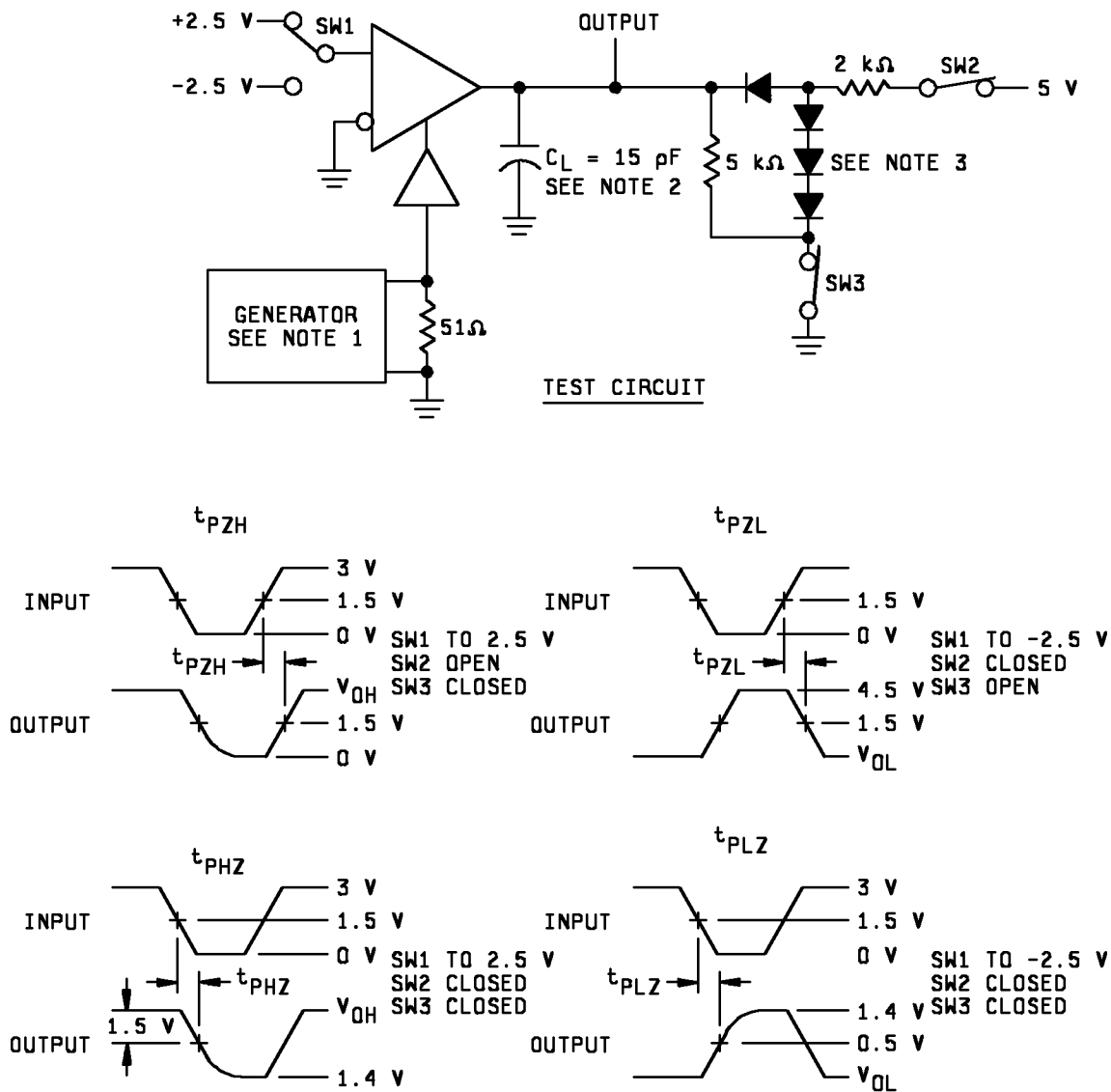
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NOTES:

1. The input pulse is supplied by a generator having the following characteristics: $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, duty cycle 50%, $Z_{OUT} = 50 \text{ } \Omega$.
2. C_L includes probe and stray capacitance.
3. All diodes are 1N3064 or equivalent.

FIGURE 4. Test circuit and switching waveforms - continued.

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TABLE II. Electrical test requirements .

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed
to the limits specified in table I.

4.3 Quality conformance inspection . Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection .

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections .

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544. d

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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